

#3/12-7-01
Date

S/N Unknown

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Applicant: | Christophe J. Chevallier | Examiner: | Unknown |
| Serial No.: | Unknown | Group Art Unit: | Unknown |
| Filed: | Herewith | Docket: | 703.019US3 |
| Title: | SUPPLY VOLTAGE REDUCTION CIRCUIT FOR INTEGRATED CIRCUIT | | |



INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for review in connection with the above-identified patent application. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner be returned to the Applicant.

In accordance with 37 C.F.R. § 1.98(d), copies of the listed documents are not provided as these references were previously cited by or submitted to the U.S. Patent Office in connection with Applicant's prior U.S. application, Serial No. 09/448,881, filed on November 24, 1999, which is relied upon for an earlier filing date under 35 U.S.C. § 120.

Applicant respectfully request consideration of these references during prosecution of the above-identified matter. The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

CHRISTOPHE J. CHEVALLIER

By his Representatives,

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9/18/2001

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Date of Deposit: September 18, 2001

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.